**BRAC UNIVERSITY**

**Department of Computer Science and Engineering**

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| Examination: Midterm (**Section-5**)  Duration: 1 hour | Semester: Spring-20  Full Marks: 30 |

CSE 340: Computer Architecture

[Answer the following questions.

Figures in the right margin indicate marks.

Write the initial of your faculty at TOP of your answer script.]

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| Name: | ID: | Section: 5 |

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| **1.(CO1)** | a. | **List** 4 major characteristics of RISC architecture. | 4 |
| b. | **Show** the diagram of a shift register that can shift both left and right, clear data and output data. | 6 |
| **2.(CO1)** | a. | **Define** throughput and ISA. | 2 |
|  | b. | Suppose a program is running on a PC with 3.2Ghz AMD Ryzen 5 processor. The program consists of 3 major types of instructions. Their instruction counts and CPI are given below:   |  |  |  | | --- | --- | --- | | **Instruction Type** | **Instruction Count(x109)** | **CPI** | | Load/Store | 3 | 2.3 | | Matrix Multiplication | 5 | ? | | Add/Subtraction | 2 | 2.0 |   If the average CPI of the program is 6.3 then **what** is he CPI of the Matrix Multiplication Instruction? | 3 |
| **3.(CO2)** | a. | **Construct** the equivalent MIPS code of the following C code.  For(i=5;i>0;i--)  {  if (A[i] != i)  F[5] = A[F[5]]  }  **Hints:** Consider base addresses of array A and F are in register $10 and $11. Also consider *i* is in register $8. **Also, you can use any register from $1 to $31 for intermediate calculations.** | 6 |
|  | b. | **Show** the encoding of the following MIPS instructions with specifying the instruction type (R/I/J).  I**. BNE $1,$5,5**   II. **BGE $2,$12,10**  III. **SRL $6,$4,3**   IV. **SUB $7,$8,$9** | 4 |
| **4 (CO2)** |  | **Identify** the decimal floating point number that is represented by 0xBC4D0000. You have to show the whole process. | 5 |